November 2005

FDS8960C

Dual N & P-Channel PowerTrench® MOSFET

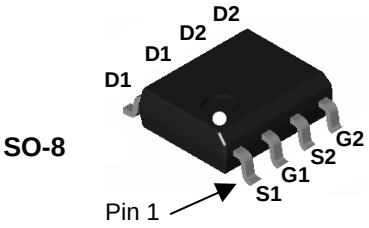
General Description

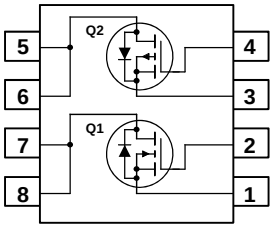
These dual N- and P-Channel enhancement mode power field effect transistors are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state ressitance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Features

- **Q1**: N-Channel
  7.0A, 35V $R_{DS(on)}$ = 0.024Ω @ V_{GS} = 10V
  $R_{DS(on)}$ = 0.032Ω @ V_{GS} = 4.5V
- **Q2**: P-Channel
  –5A, –35V $R_{DS(on)}$ = 0.053Ω @ V_{GS} = –10V
  $R_{DS(on)}$ = 0.087Ω @ V_{GS} = –4.5V
- Fast switching speed
- RoHS compliant





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V_{DSS}	Drain-Source Voltage		35	–35	V
$V_{DS(Avalanche)}$	Drain-Source Avalanche Voltage (maximum)	(Note 3)	40	–40	V
V_{GSS}	Gate-Source Voltage		±20	±25	V
I_D	Drain Current - Continuous	(Note 1a)	7	–5	A
	- Pulsed		20	–20	
P_D	Power Dissipation for Dual Operation		2		W
	Power Dissipation for Single Operation	(Note 1a)	1.6		
		(Note 1b)	1		
		(Note 1c)	0.9		
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS8960C	FDS8960C	13"	12mm	2500 units

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Avalanche Ratings							
E_{AS}	Drain-Source Avalanche Energy (Single Pulse)	V_{DD} = 35 V, I_D = 7 A, L = 1 mH	Q1			24.5	mJ
		V_{DD} = –35 V, I_D =–5 A, L = 1 mH	Q2			12.5	mJ
I_{AS}	Drain-Source Avalanche Current		Q1 Q2		7 –5		A
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA V_{GS} = 0 V, I_D = –250 μA	Q1 Q2	35 –35			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C I_D = –250 μA, Referenced to 25°C	Q1 Q2		31 –40		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 28 V, V_{GS} = 0 V V_{DS} = –28 V, V_{GS} = 0 V	Q1 Q2			1 –1	μA
I_{GSSF}	Gate-Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V	Q1			100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	V_{GS} = –20 V, V_{DS} = 0 V				–100	nA
I_{GSSR}	Gate-Body Leakage, Forward	V_{GS} = 25 V, V_{DS} = 0 V	Q2			100	nA
I_{GSSF}	Gate-Body Leakage, Reverse	V_{GS} = –25 V, V_{DS} = 0 V				–100	nA
On Characteristics (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA V_{DS} = V_{GS}, I_D = –250 μA	Q1 Q2	1 –1	2 –1.8	3 –3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C I_D = –250 μA, Referenced to 25°C	Q1 Q2		–5 4		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 7 A V_{GS} = 4.5 V, I_D = 6 A V_{GS} = 10 V, I_D = 7 A, T_J = 125°C	Q1		20 25 29	24 32 37	mΩ
		V_{GS} = –10 V, I_D = –5 A V_{GS} = –4.5 V, I_D = –4 A V_{GS} = –10 V, I_D = –5 A, T_J = 125°C	Q2		44 70 61	53 87 79	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 7 A V_{DS} = –5 V, I_D =–5 A	Q1 Q2		23 9		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	Q1 V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz	Q1 Q2		570 540		pF
C_{oss}	Output Capacitance	Q2 V_{DS} = –15 V, V_{GS} = 0 V, f = 1.0 MHz	Q1 Q2		126 113		pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		52 60		pF
R_G	Gate Resistance	f = 1.0 MHz	Q1 Q2		2 6		Ω

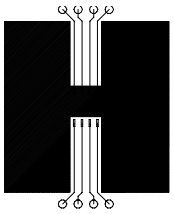
Electrical Characteristics (continued)

T_A = 25°C unless otherwise noted

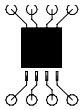
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Switching Characteristics (Note 2)							
$t_{d(on)}$	Turn-On Delay Time	Q1 V_{DD} = 15 V, I_D = 1 A, V_{GS} = 10V, R_{GEN} = 6 Ω	Q1 Q2		8 12	16 22	ns
t_r	Turn-On Rise Time		Q1 Q2		5 16	10 29	ns
$t_{d(off)}$	Turn-Off Delay Time	Q2 V_{DD} = –15 V, I_D = -1 A, V_{GS} = –10V, R_{GEN} = 6 Ω	Q1 Q2		23 20	37 32	ns
t_f	Turn-Off Fall Time		Q1 Q2		3 5	6 10	ns
Q_g	Total Gate Charge	Q1 V_{DS} = 15 V, I_D = 7 A, V_{GS} = 5 V	Q1 Q2		5.5 5.7	7.7 8	nC
Q_{gs}	Gate-Source Charge	Q2 V_{DS} = –15 V, I_D = –5 A, V_{GS} = –5 V	Q1 Q2		1.8 1.8		nC
Q_{gd}	Gate-Drain Charge		Q1 Q2		1.8 2		nC
Drain–Source Diode Characteristics							
I_S	Maximum Continuous Drain-Source Diode Forward Current		Q1 Q2			1.3 –1.3	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.3 A (Note 2) V_{GS} = 0 V, I_S = –1.3 A (Note 2)	Q1 Q2		0.8 –0.8	1.2 –1.2	V
t_{rr}	Diode Reverse Recovery Time	Q1 I_F = 7 A, d_{iF}/d_t = 100 A/µs	Q1 Q2		20 17		nS
Q_{rr}	Diode Reverse Recovery Charge	Q2 I_F = -5 A, d_{iF}/d_t = 100 A/µs	Q1 Q2		10 5		nC

Notes:

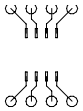
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C/W when mounted on a 0.5 in^2 pad of 2 oz copper



b) 125°C/W when mounted on a .02 in^2 pad of 2 oz copper



c) 135°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

3. BV(avalanche) Single-Pulse rating is guaranteed by design if device is operated within the UIS SOA boundary of the device.

Typical Characteristics: Q1 (N-Channel)

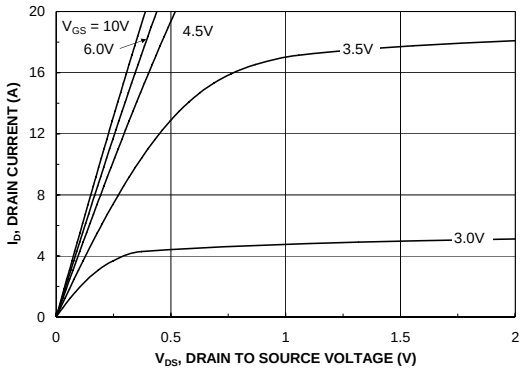


Figure 1. On-Region Characteristics.

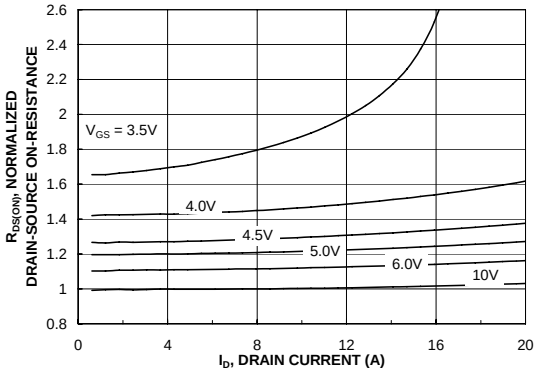


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

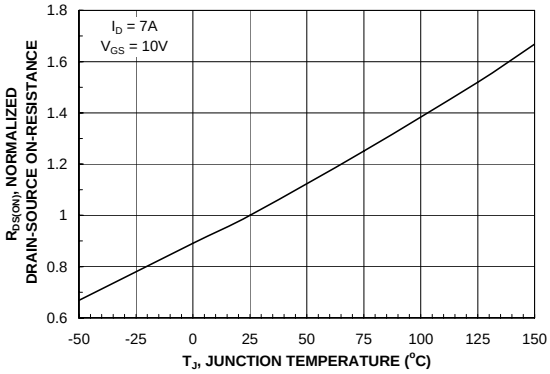


Figure 3. On-Resistance Variation with Temperature.

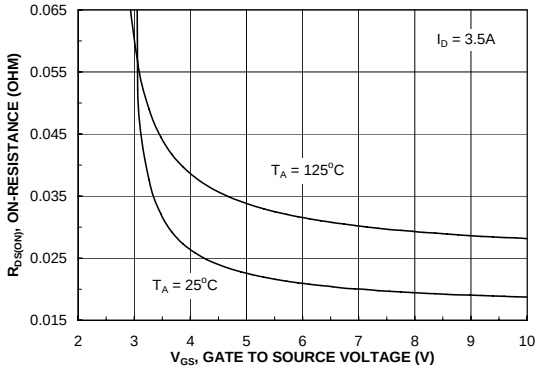


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

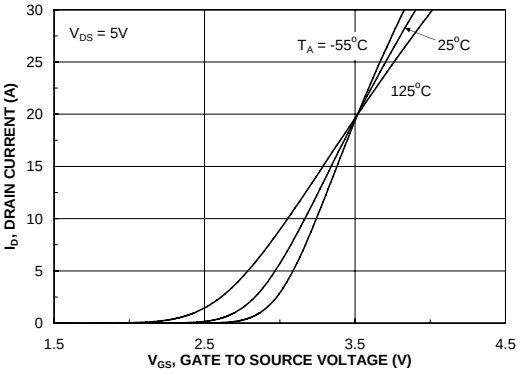


Figure 5. Transfer Characteristics.

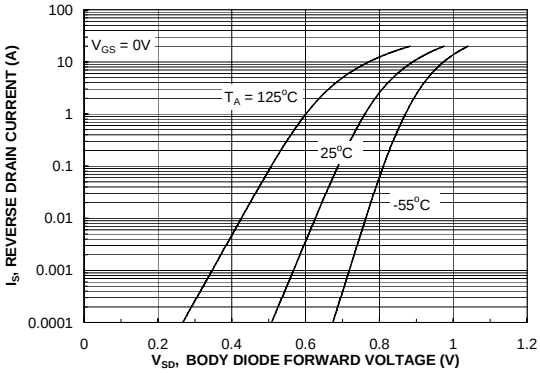


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q1 (N-Channel)

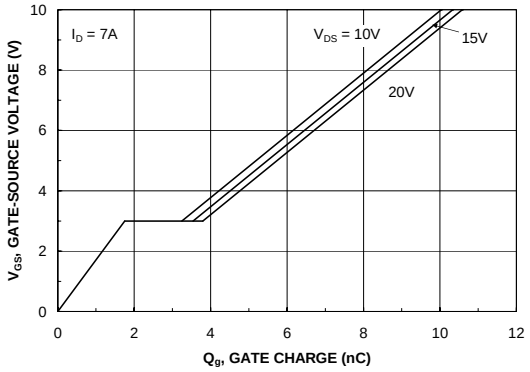


Figure 7. Gate Charge Characteristics.

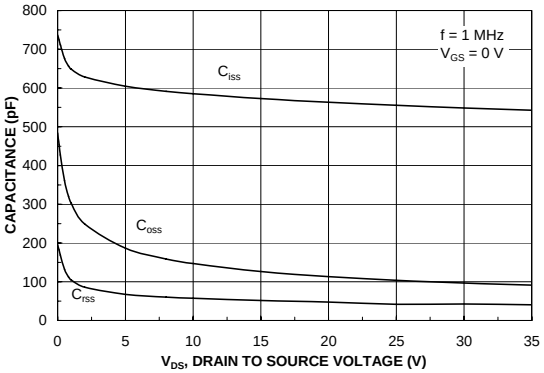


Figure 8. Capacitance Characteristics.

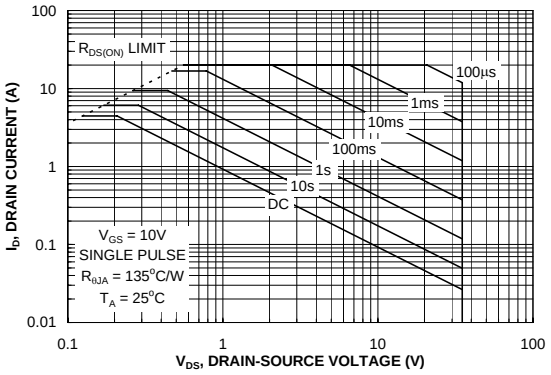


Figure 9. Maximum Safe Operating Area.

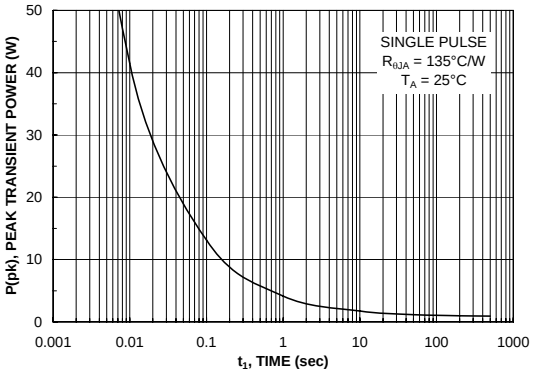


Figure 10. Single Pulse Maximum Power Dissipation.

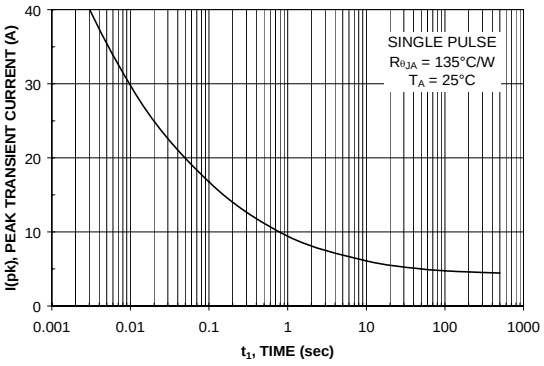


Figure 11. Single Pulse Maximum Peak Current

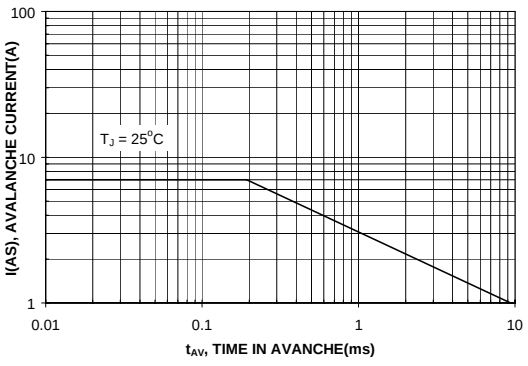


Figure 12. Unclamped Inductive Switching Capability

Typical Characteristics: Q2 (P-Channel)

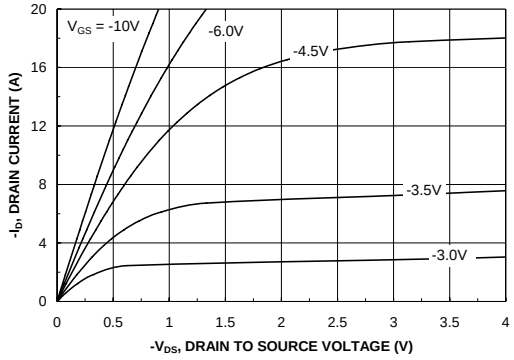


Figure 13. On-Region Characteristics.

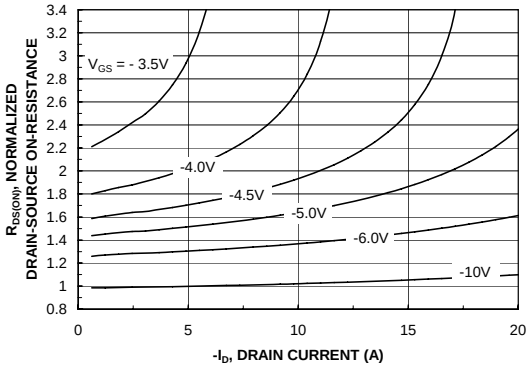


Figure 14. On-Resistance Variation with Drain Current and Gate Voltage.

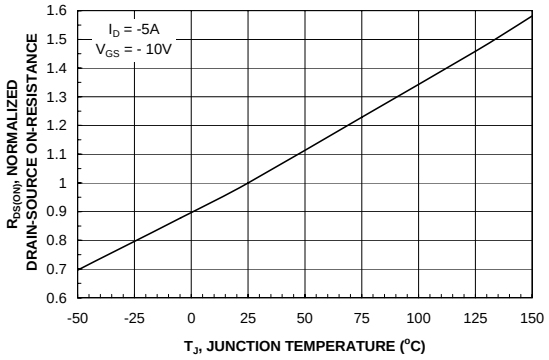


Figure 15. On-Resistance Variation with Temperature.

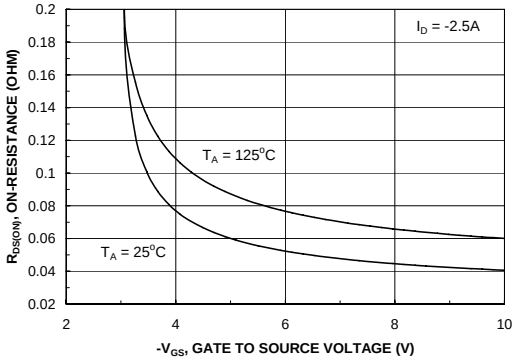


Figure 16. On-Resistance Variation with Gate-to-Source Voltage.

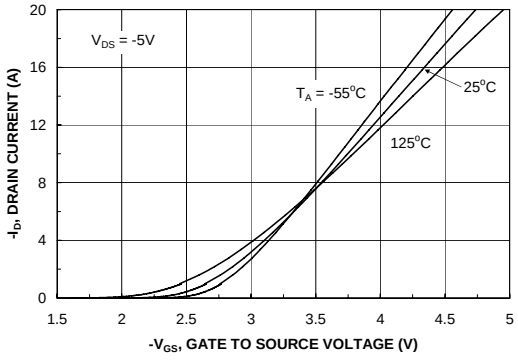


Figure 17. Transfer Characteristics.

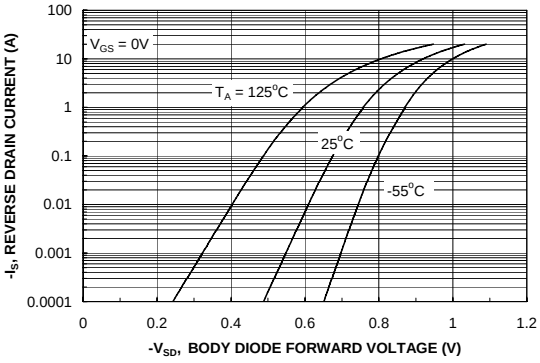


Figure 18. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q2 (P-Channel)

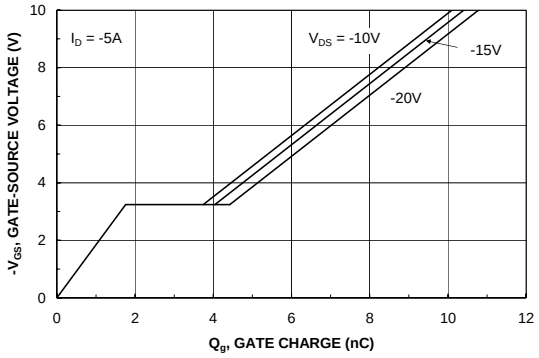


Figure 19. Gate Charge Characteristics.

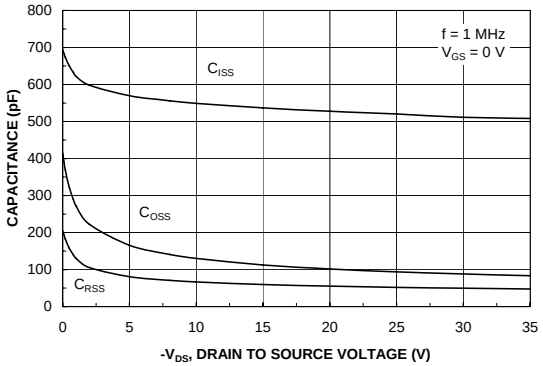


Figure 20. Capacitance Characteristics.

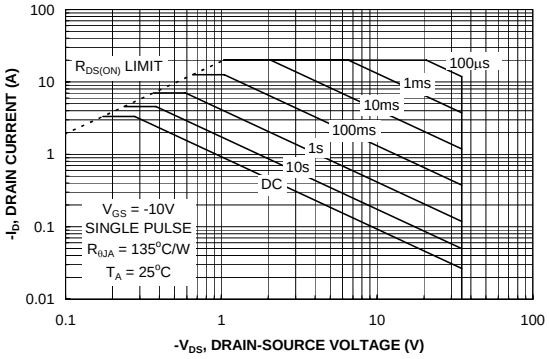


Figure 21. Maximum Safe Operating Area.

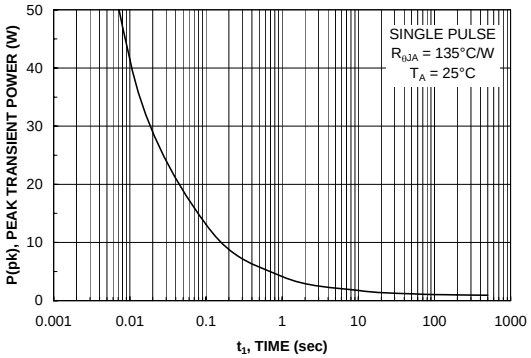


Figure 22. Single Pulse Maximum Power Dissipation.

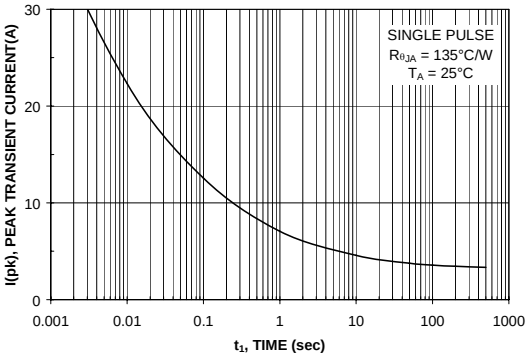


Figure 23. Single Pulse Maximum Peak Current

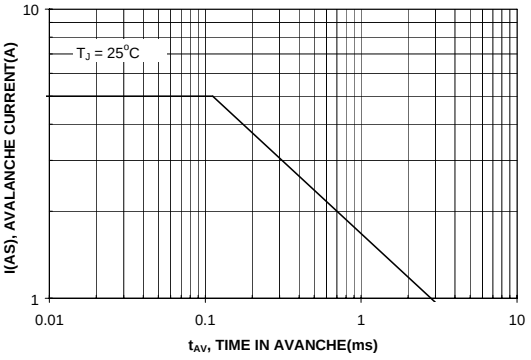


Figure 24. Unclamped Inductive Switching Capability

Typical Characteristics

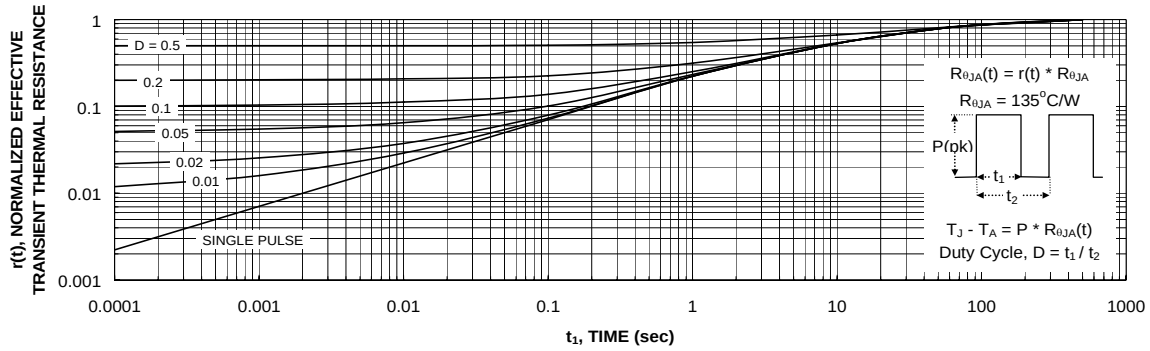


Figure 25. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.